FIG. 1

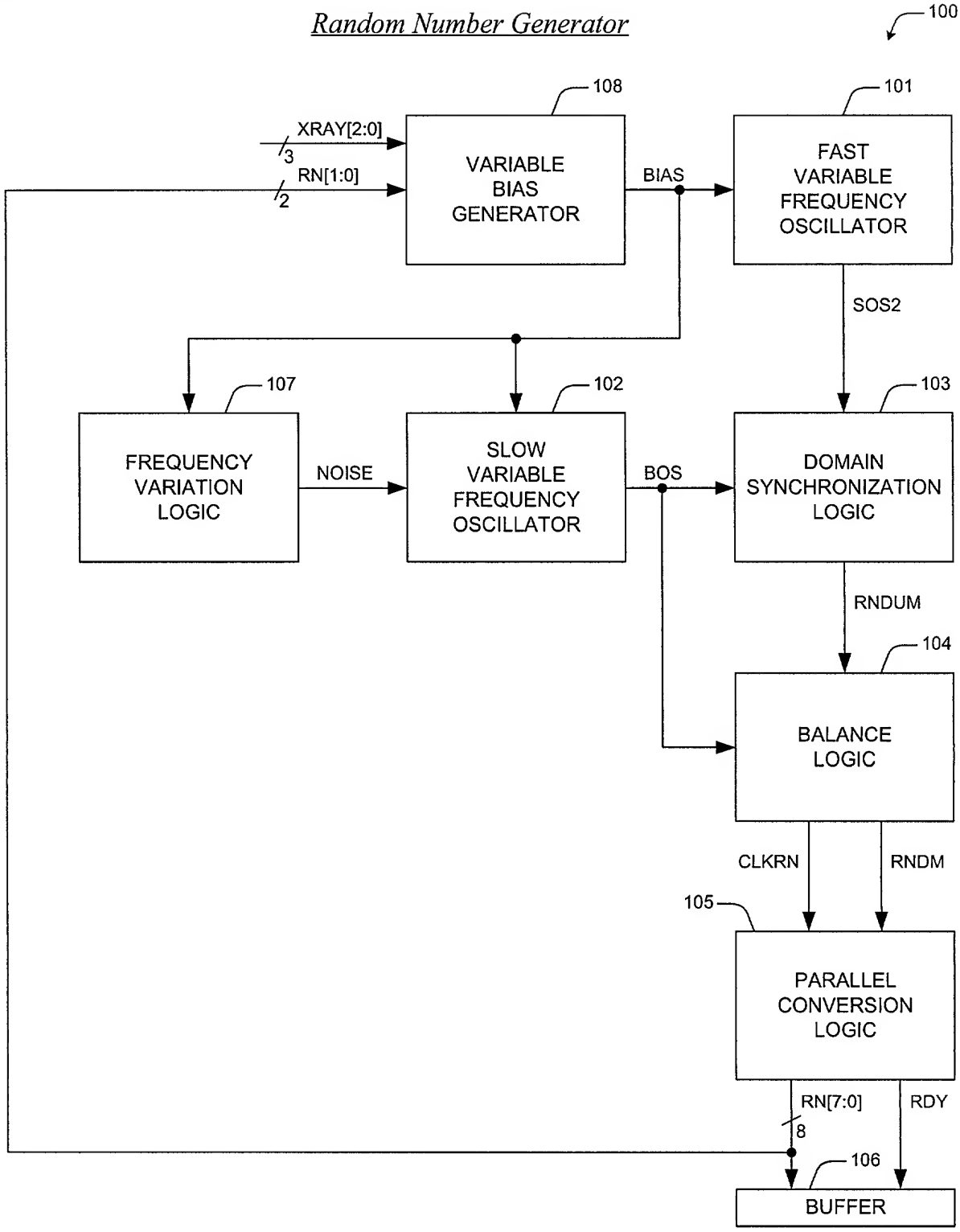
Random Number Generator
100
108
101
XRAY[2:0]
3
RN[1:0]
2
VARIABLE BIAS GENERATOR
BIAS
FAST VARIABLE FREQUENCY OSCILLATOR
SOS2
107
102
103
FREQUENCY VARIATION LOGIC
NOISE
SLOW VARIABLE FREQUENCY OSCILLATOR
BOS
DOMAIN SYNCHRONIZATION LOGIC
RNDUM
104
BALANCE LOGIC
CLKRN
RNDM
105
PARALLEL CONVERSION LOGIC
RN[7:0]
8
RDY
106
BUFFER

FIG. 2

200

Variable Bias Control of Oscillators

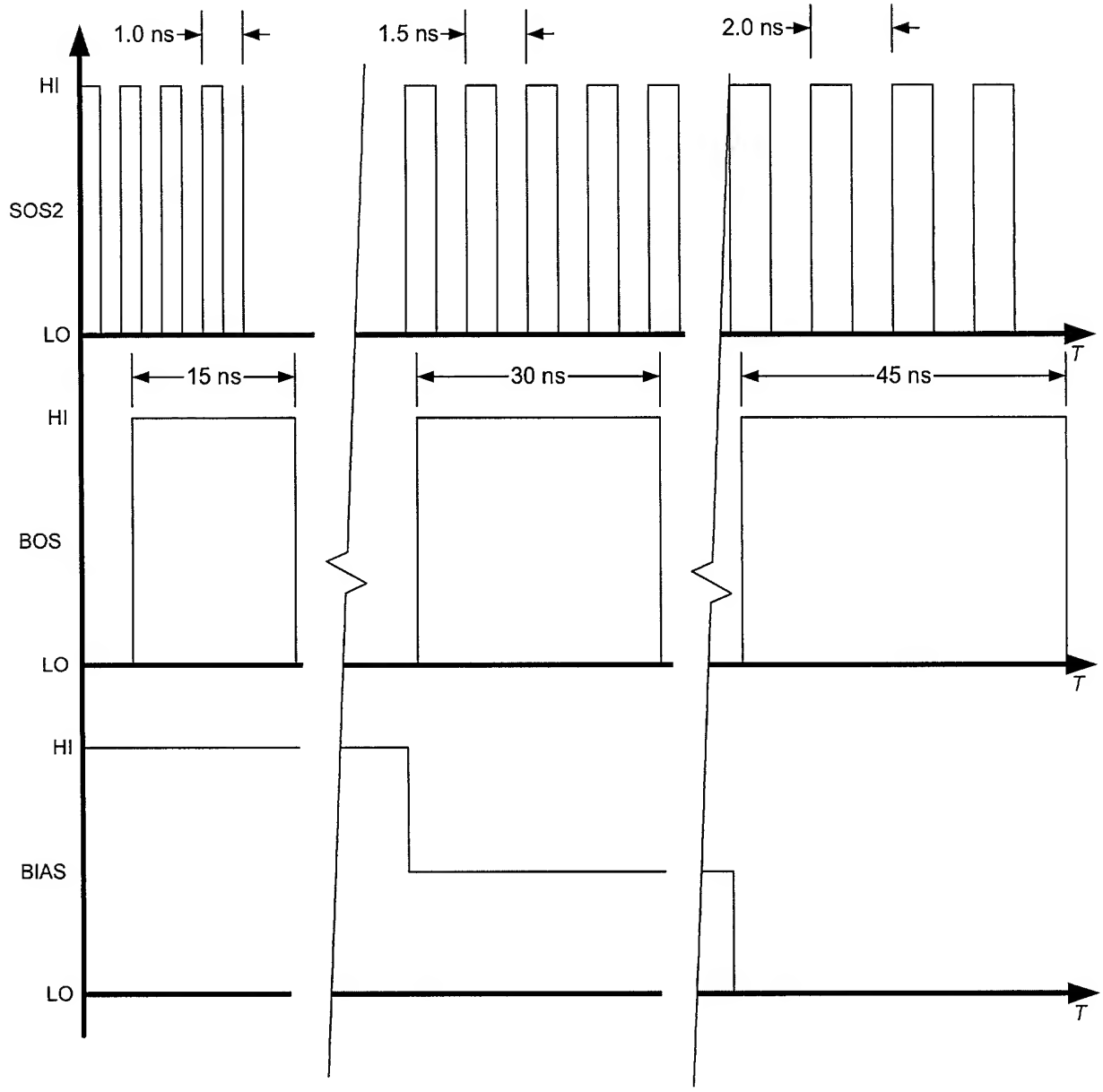

FIG. 3

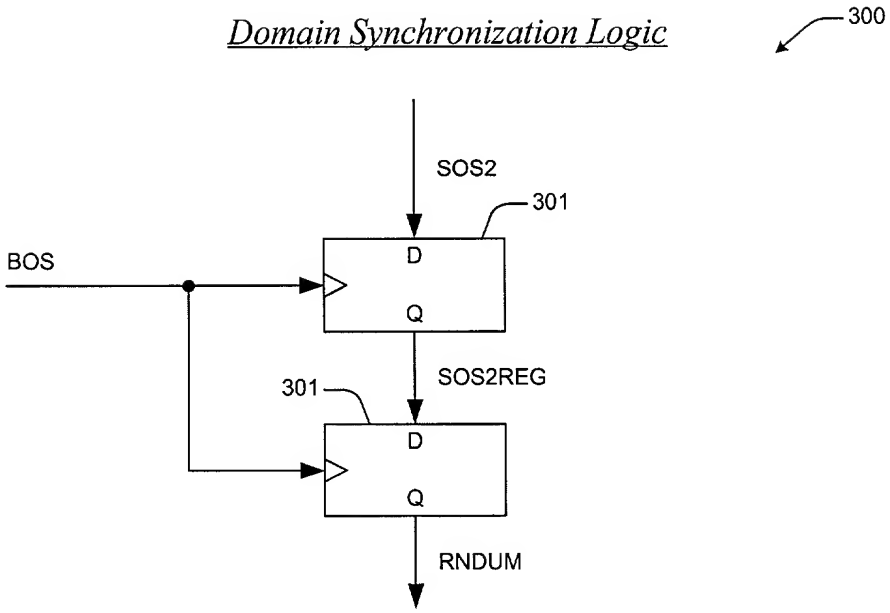
Domain Synchronization Logic
300
SOS2
301
BOS
D
Q
SOS2REG
301
D
Q
RNDUM

FIG. 4

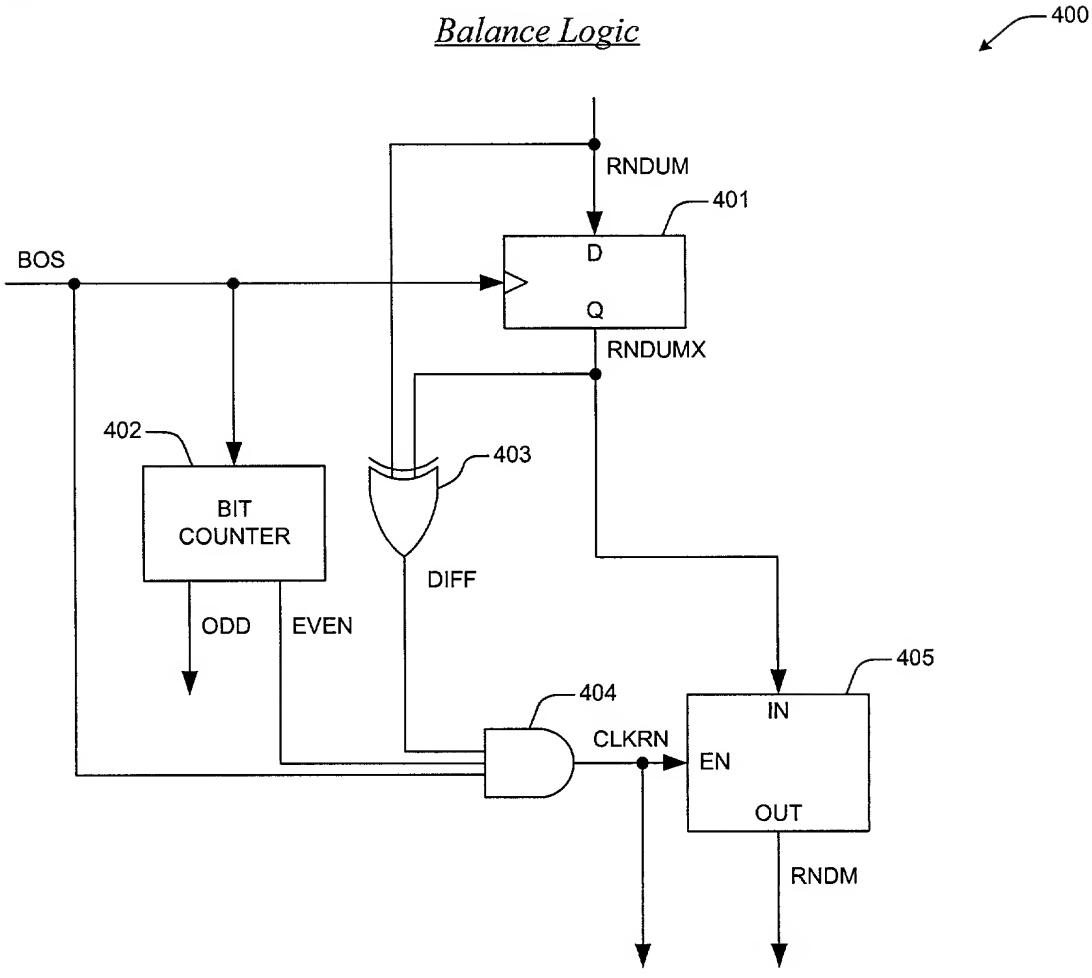
Balance Logic
400
RNDUM
401
BOS
D
Q
RNDUMX
402
403
BIT
COUNTER
DIFF
ODD
EVEN
405
404
IN
CLKRN
EN
OUT
RNDM

FIG. 5

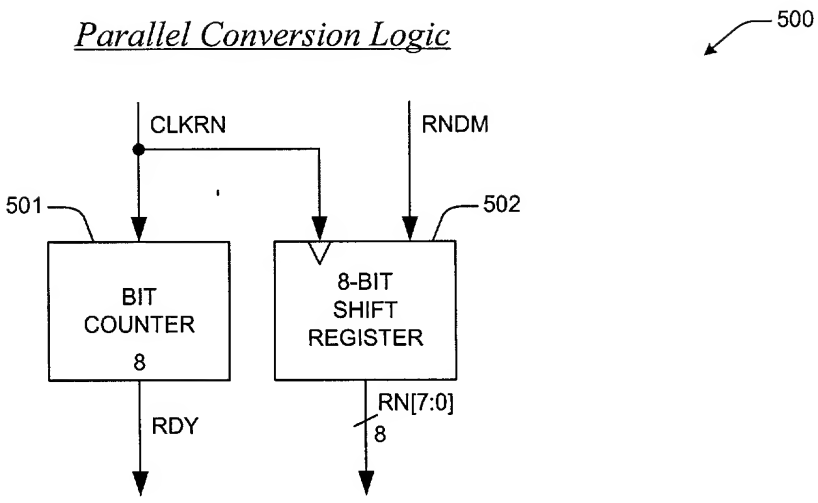
Parallel Conversion Logic
500
CLKRN
RNDM
501
502
BIT
COUNTER
8
8-BIT
SHIFT
REGISTER
RDY
RN[7:0]
8

FIG. 6

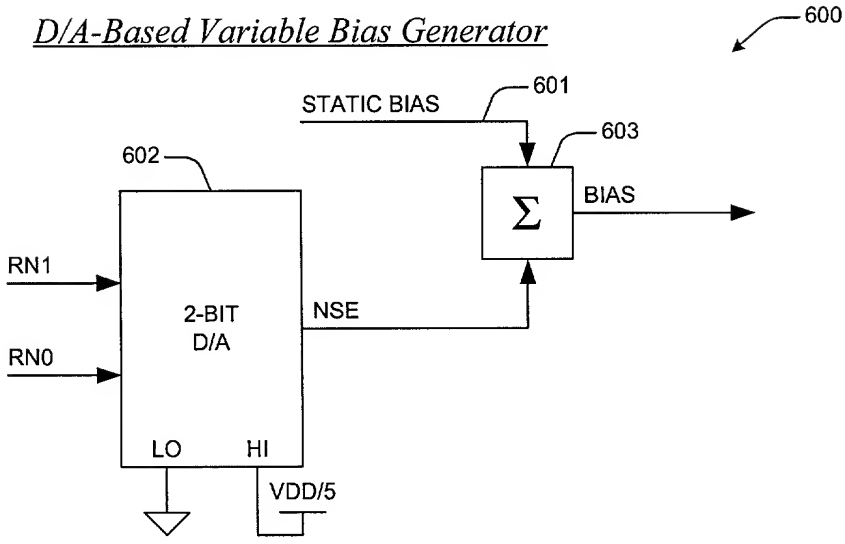
D/A-Based Variable Bias Generator
600
STATIC BIAS
601
603
602
BIAS
Σ
RN1
2-BIT
D/A
NSE
RN0
LO
HI
VDD/5

FIG. 7

Device-Based Variable Bias Generator

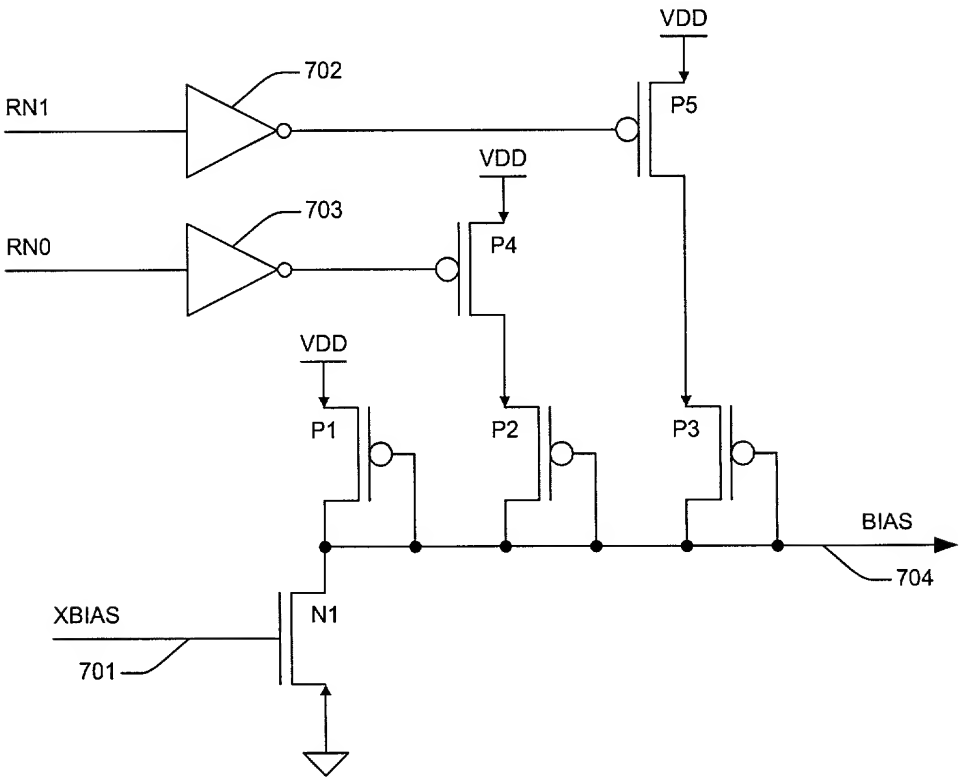

FIG. 8

Slow Frequency Variation Logic

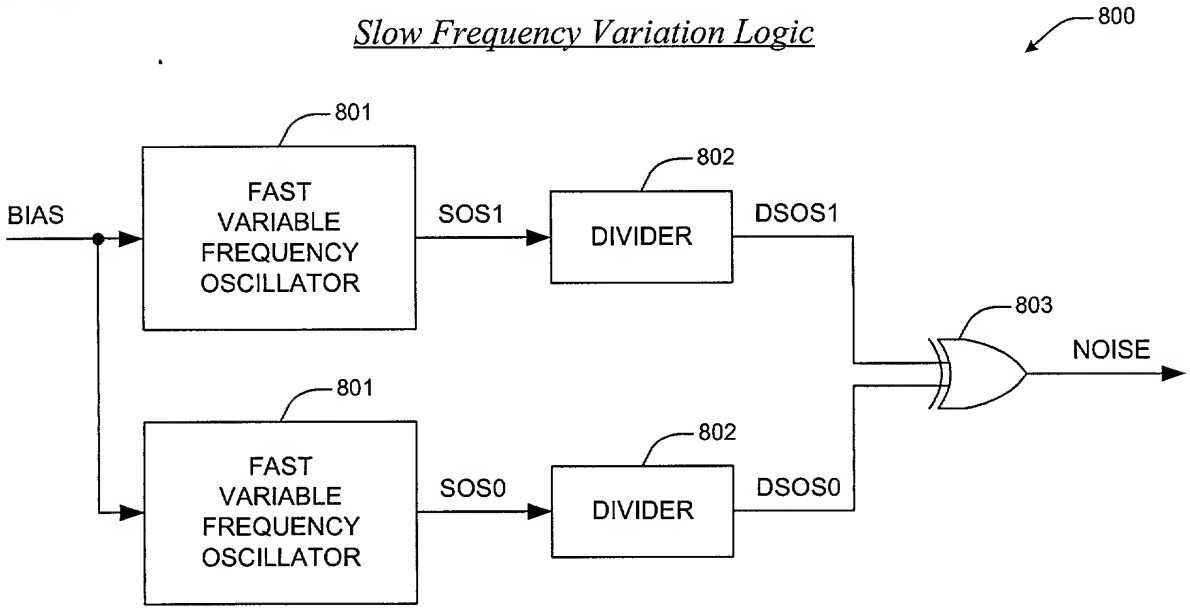

FIG. 9

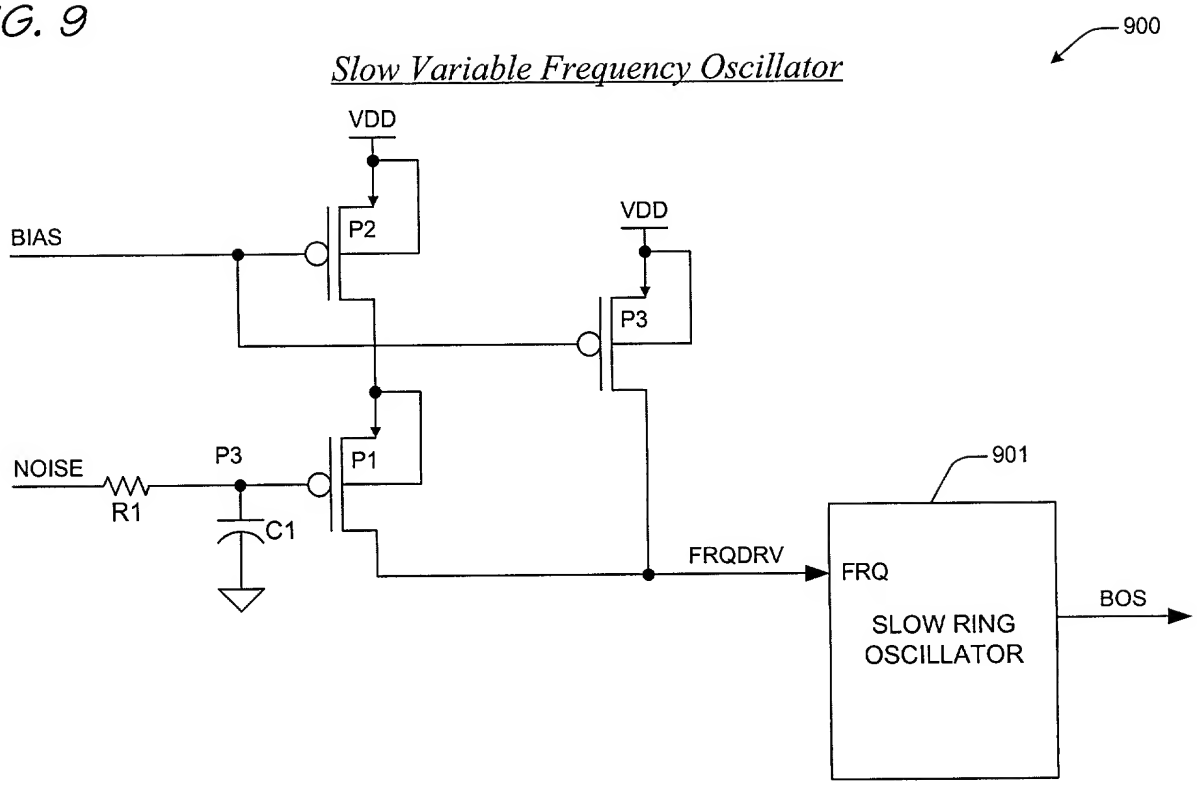
900
Slow Variable Frequency Oscillator
VDD
BIAS
P2
VDD
P3
NOISE
P3
P1
R1
C1
901
FRQDRV
FRQ
SLOW RING
OSCILLATOR
BOS

FIG. 10

Fast Oscillator Frequency

1000

XRAY[2:0]	BIAS (mv)	SOS_PERIOD (ns)	SOS_FREQUENCY
100	766	2.00	(MHz)
101	750	1.88	500
110	736	1.80	532
111	717	1.70	556
000	694	1.61	588
001	668	1.46	621
010	594	1.30	685
011	509	1.15	769
			870

FIG. 11

Slow Oscillator Frequency

1100

XRAY[2:0]	BIAS (mv)	NOISE = 0		NOISE = 1	
		BOS PERIOD (ns)	BOS FREQUENCY (MHz)	BOS PERIOD (ns)	BOS FREQUENCY (MHz)
100	766	20.0	50	46.0	22
101	750	19.0	53	44.0	23
110	736	18.0	56	42.8	23
111	717	17.3	58	33.5	30
000	694	17.0	59	31.9	31
001	668	16.4	61	31.0	32
010	594	16.1	62	28.0	36
011	509	15.8	63	25.8	39